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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/568,666	01/21/2008	Tomoyoshi Sato	29898/40913	5116

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EXAMINER

TREAT, WILLIAM M

ART UNIT	PAPER NUMBER
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2181

NOTIFICATION DATE	DELIVERY MODE
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04/12/2011

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mgbdocket@marshallip.com

Office Action Summary

Application No.

10/568,666

Applicant(s)

SATO, TOMOYOSHI

Examiner

William M. Treat

Art Unit

2181

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 January 2011.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 2 and 4-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 2 and 4-34 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 January 2011 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-945)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

1. Claims 1-2 and 4-34 are presented for examination.
2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2 and 4-34 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Snyder (Patent No. 6,507,214).
4. The reasons, given in the examiner's previous action for rejecting claims 1-2 and 4-34, continue and are hereby incorporated by reference.
5. Applicant first argues on behalf of claims 1, 2, 4-11, and 13-29 that: "In particular, Snyder describes an already structured programmable digital circuit block 100, which includes programmable configuration registers 50. Snyder only describes programming its registers 50 via a bus 90. (Snyder, col. 3, lines 3-18.) Snyder does not provide any solution as to how to divide circuits onto a region. Snyder does not describe mapping the object circuit and the interface circuit in contact with the object circuit onto the logic circuit region according to the object circuit information and the interface circuit information, as recited in claims 1, 9, 26, and 28."
6. The examiner would first point out Snyder's Fig. 2 represents an embodiment of his invention which is a large logic circuit (200) made up of multiple, smaller logic circuits (100). An object circuit can be mapped onto a region of the larger circuit (200) depicted in Fig. 2 which includes multiple smaller logic circuits (100) (col. 4, line 61 through col. 5, line 18 and col. 6, lines 39-50). Inherent in the tasks described by

Snyder are the mapping of the object circuit and interface circuit based on object circuit information and interface circuit information. Randomly configuring logic circuits (100) in circuit (200) and failing to properly connect/interface the logic circuits would not result in an operational device and an assumption before the law is that the device described by a patent is operable.

7. Applicant next argues: "With respect to claims 30-34, of which claim 30 is the independent claim to which claims 31-34 depend, Snyder does not describe or suggest at least, 'the [reconfigurable] elements [of the logic circuit, which] respectively include an operation core that performs a logic operation on input data and outputs output data, the operation core including a selector into which a multibit function code for designating the logic operation is inputted and which selects the output data according to the input data.'" As to claim 30, the examiner would point to col. 3, line 66 through col. 4, line 7 of Snyder where he taught, for example, the logic circuit 100, when its configuration register is programmed by a multibit function code (i.e., configuration data) which designates the logic operation necessary for a CRC checker or CRC generator, would select the output data according to the input data.

8. It is incumbent upon the examiner to give applicant's claim language its broadest reasonable interpretation. The invention of applicant's broad claim language does not distinguish over Snyder.

9. Applicant's arguments filed 1/14/2011 have been fully considered but they are not persuasive. See the preceding paragraphs of the examiner's rejection.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/William M. Treat/
Primary Examiner, Art Unit 2181